SEGMENT BUFFER LOADING IN A DEINTERLACER

Clyde H. Nagakura
Qinggang Zhou
Thomas M. Chan

ABSTRACT OF THE DISCLOSURE:

A display processor integrated circuit includes a display processor portion and an on-chip programmable logic portion. The programmable logic portion can be configured to implement custom video and/or image enhancement functions. The display processor portion performs block-based motion detection. If no motion is detected for a given block of pixels, then interline gaps in the block are filled using temporal interpolation. If motion is detected, then interline gaps are filled using spatial interpolation. To maintain accuracy without unduly increasing computational complexity, a less complex high angle spatial interpolation method is employed where a low angle tilt condition is not detected. A more computationally intensive low angle spatial interpolation method can therefore be employed in low angle tilt conditions. Integrated circuit cost is reduced by employing pipelining to write parts of segment buffers at the same time that other parts are being read to perform the interpolation process.